Features

- 3 input reference clocks:
  - Two differential clock pairs supporting up to 3.1GHz and accepting single-ended clock source
  - One crystal input,accepting 8MHz to 50MHz crystal or single-ended clock source
- 10 output clocks:
  - Two power banks with 5 differential outputs each,supporting LVPECL,LVDS and LP_HCSL
  - One independent LVCMOS output clock
- Frequency range:
  - LVCMOS:DC to 350MHz
  - LVDS:DC to 3.1GHz
  - LVPECL:DC to 3.1GHz
  - LP-HCSL:DC to 1GHz
- Excellent Power Supply Ripple Rejection(PSRR)
- Ultra-low latency and skew
- Three independently configurable 1.8V-3.3V power supplies for:
  - Differential outputs
  - Single-ended outputs
  - Core
- Pin-based control,allowing input reference selection,output I/O type selection and output enable/disable
- Working Temperature: -40°C to +85 °C
- Package:48-pin WQFN,7mm x 7mm

Note：

1、SYKB*****: No glitch-free switchover.

2、SYKB*****G: Includes glitch-free switchover

3、Unless otherwise stated, the terms "clock buffer" or "buffer" refer to the entire series.

General Description

SYKB23F10/SYKB23F10(G) is a 3.1GHz high-performance clock fanout buffer with 10 outputs, designed for low-jitter,high-frequency clock/ data distribution and level translation.

The buffer supports clock input selection from either two differential clocks or a crystal input,distributing the selected clock to two output banks,each with five differential outputs,plus one LVCMOS output. Both differential output banks can be configured as LVPECL,LVDS,LPHSCL,or disabled.

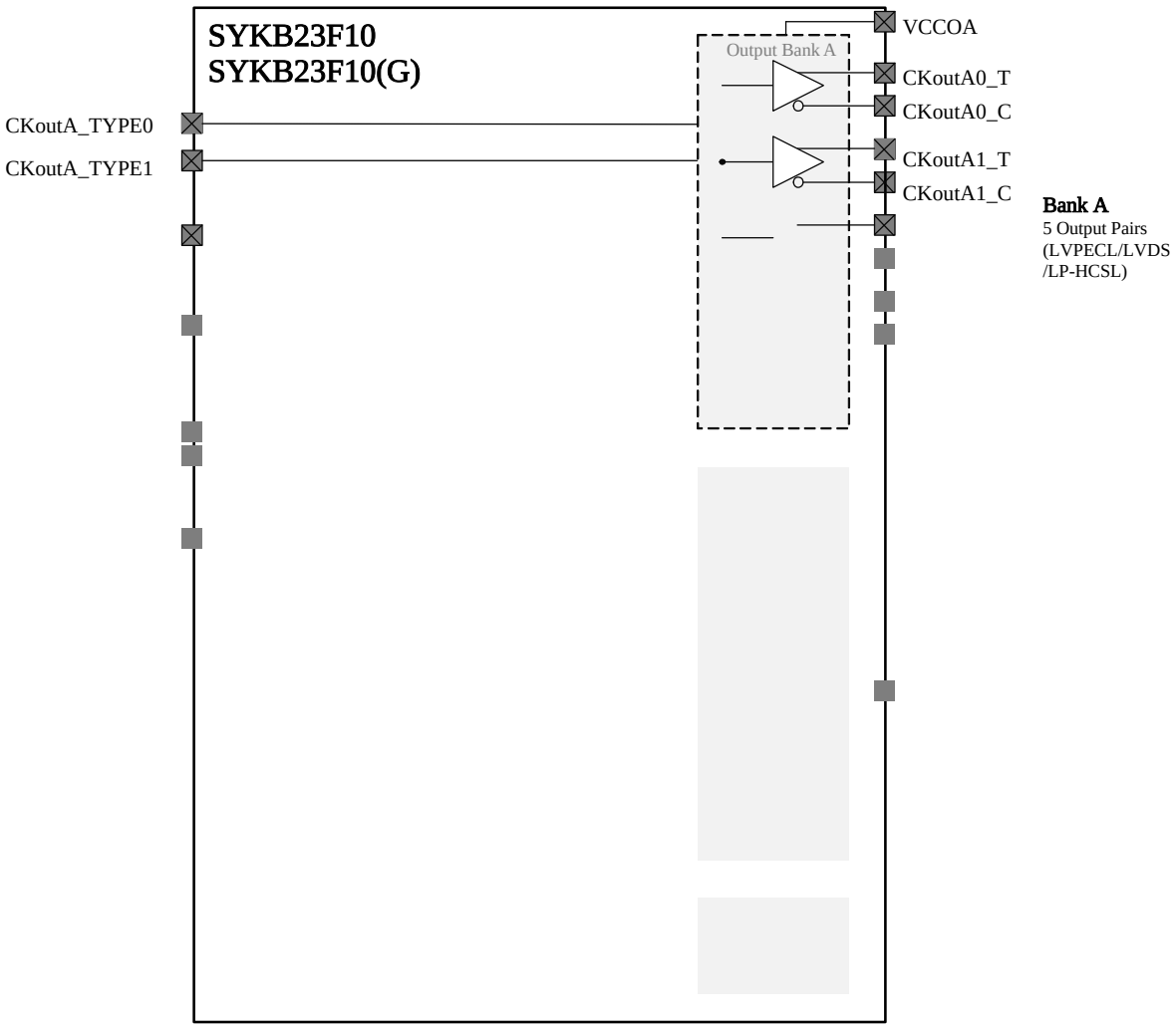
Operating on a core supply of 1.8V-3.3V and three independent output supplies of 1.8V-3.3V, SYKB23F10 provides flexible control via logic pins for input reference selection,differential I/O type selection,and output enable/disable functions.

The buffer can be paired with SYNK clock generator SYKG10XX for an effective clock tree solution. Overall,SYKB23F10 offers competitive input reference and output frequency ranges,power strategy,and propagation delaywhile supporting a wider working temperature range.

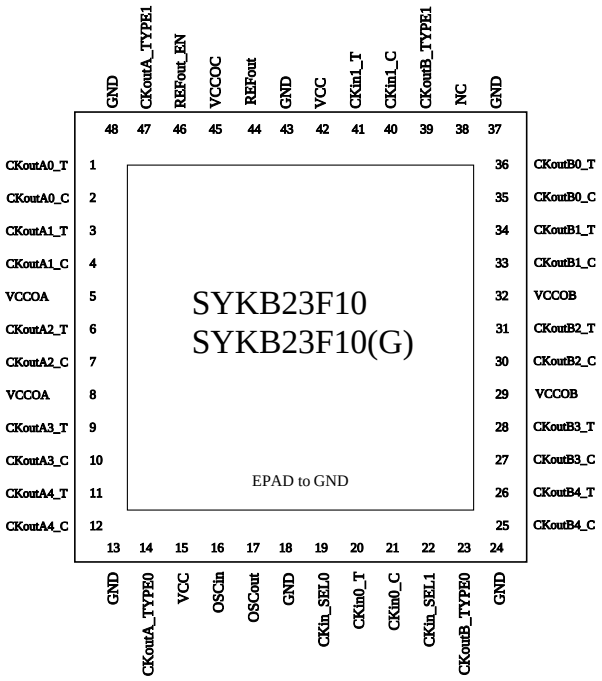
Applications

- Clock distribution and level translation for ADCs, DACs,SATA/SAS,SONET/SDH,multi-gigabit ethernet,and fiber channel line cards
- Servers,storages,switches,routers,and display panels
- PCIe 1.0 to 6.0 and NVLink
- Reference clock distribution for BBU and RRU applications

Functional Block Diagram



Pin Assignment (48-pin WQFN)



Ordering Information

Part Number	Package	Operating Temperature
SYKB23F10	48-pin WQFN, 7.0mm x 7.0mm x 0.75mm	-40°C to +85°C
SYKB23F10(G)		

For more information on the product, please contact https://www.yxc.hk.